WHAT IS CLAIMED IS:

1. A method for optimizing relationships between logic commands defining a circuit design input to an analysis tool, the method comprising:

responsive to a determination that a value of logic level of a signal can be inferred:

responsive to an attempt by the analysis tool to set the logic level of the signal to a calculated value, determining whether the calculated value is equal to the inferred value; and

if the calculated value is equal to the inferred value, setting the logic level of the signal to the inferred value.

2. The method of claim 1 further comprising:

if the calculated value is not equal to the inferred value, preventing the analysis tool from setting a logic level of the signal.

3. The method of claim 2 further comprising, responsive to the preventing, generating an error message indicating that a logic level of the signal has not been set.

4. The method of claim 1 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto.

5. A method for optimizing relationships between logic commands defining a circuit design input to an analysis tool, the method comprising:

responsive to a determination that a value of logic level of a signal can be inferred:

responsive to an attempt by the analysis tool to set the logic level of the signal to a calculated value, determining whether the calculated value is equal to the inferred value;

if the calculated value is equal to the inferred value, setting the logic level of the signal to the inferred value; and

if the calculated value is not equal to the inferred value, refraining from setting a logic level of the signal.

6. The method of claim 5 further comprising, responsive to the refraining, generating an error message, wherein the error message indicates that a logic level of the signal has not been set.

7. The method of claim 5 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto.

8. A circuit analysis tool for optimizing relationships between logic commands defining a circuit design input to the tool, the tool comprising:

means responsive to a determination that a value of logic level of a signal can be inferred and to an attempt by the analysis tool to set the logic level of the signal to a calculated value for determining whether the calculated value is equal to the inferred value; and

means responsive to the calculated value being equal to the inferred value for setting the logic level of the signal to the inferred value.

9. The tool of claim 8 further comprising:

means responsive to the calculated value not being equal to the inferred value for preventing the analysis tool from setting a logic level of the signal.

10. The tool of claim 9 further comprising means responsive to the means for preventing for generating an error message indicating that a logic level of the signal has not been set.

11. The tool of claim 8 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto.

12. A circuit analysis tool for optimizing relationships between logic commands defining a circuit design input to the tool, the tool comprising:

means responsive to a determination that a value of logic level of a signal can be inferred and to an attempt by the analysis tool to set the logic level of the signal to a calculated value for determining whether the calculated value is equal to the inferred value;

means responsive to the calculated value being equal to the inferred value for setting the logic level of the signal to the inferred value; and

means responsive to the calculated value not being equal to the inferred value for refraining from setting a logic level of the signal.

13. The tool of claim 12 further comprising means responsive to the means for refraining for generating an error message indicating that a logic level of the signal has not been set.

14. The tool of claim 12 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto.

15. A computer-readable medium operable with a computer for optimizing relationships between logic commands defining a circuit design input to an analysis tool, the medium having stored thereon:

computer-executable instructions responsive to a determination that a value of logic level of a signal can be inferred and to an attempt by the analysis tool to set the logic level of the signal to a calculated value for determining whether the calculated value is equal to the inferred value; and

computer-executable instructions responsive to the calculated value being equal to the inferred value for setting the logic level of the signal to the inferred value.

16. The medium of claim 15 further having stored thereon:

computer-executable instructions responsive to the calculated value not being equal to the inferred value for preventing the analysis tool from setting a logic level of the signal.

17. The medium of claim 16 further having stored thereon computer-executable instructions responsive to the preventing for returning an error message indicating that a logic level of the signal has not been set.

18. The medium of claim 15 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto.

19. A computer-readable medium operable with a computer for optimizing relationships between logic commands defining a circuit design input to an analysis tool, the medium having stored thereon:

computer-executable instructions responsive to a determination that a value of logic level of a signal can be inferred and to an attempt by the analysis tool to set the logic level of the signal to a calculated value for determining whether the calculated value is equal to the inferred value;

computer-executable instructions responsive to the calculated value being equal to the inferred value for setting the logic level of the signal to the inferred value; and

computer-executable instructions responsive to the calculated value not being equal to the inferred value for refraining from setting a logic level of the signal.

20. The medium of claim 19 further having stored thereon computer-executable instructions responsive to the refraining for generating an error message, wherein the error message indicates that a logic level of the signal has not been set.

21. The medium of claim 19 wherein a value of the logic level of the signal is inferred from logic levels of other signals of the circuit design as affected by logic commands applied thereto.